PRELIMINARY

T-52-33-05

87C75PF
MICROCONTROLLER PERIPHERAL I/O PORT EXPANDER WITH 32Kx8 EPROM

- **2 Configurable 8-bit I/O Ports**
  - **— Open Drain**
  - **— Quasi-bi-directional**
  - **— CMOS**
- **32K x 8 EPROM**
  - **— 200nS Access Time**
- **Quick-Pulse Programming™ Algorithm**
  - **— 4 Second Programming**
- **Configuration Registers**
  - **— Relocate the EPROM in Memory**
  - **— Relocate the SFRs in Memory**
  - **— Programmable RESET Level**
  - **— Double or Single Plane Operation**
- **No-Glue Microcontroller Interface**
  - **— Programmable Memory Map**
  - **— Programmable Control Signals**
  - **— Built-in Address Latches**
  - **— Integrated Address Decoder**
- **Special Function Registers (SFRs)**
  - **— Port Latch Read/Write**
  - **— Port Pin Read**
- **Low Power CHMOS-II-E**
  - **— TTL Compatible**
- **40-Pin DIP, 44-Lead PLCC**
  (See Packaging Spec., Order #231369)

The microcontroller peripheral Port Expander contains two 8-bit bi-directional I/O ports, a 32K x 8 EPROM, fully multiplexed address/data pins, and a user-configurable architecture. A microcontroller that accesses external memory must use two of its 8-bit I/O ports for multiplexed address/data lines. The Port Expander recovers these two ports while supplying needed EPROM memory. Considerable board space and design time can be saved by replacing discrete memory, port, address-decoder, address-latch, and glue chips with a single Port Expander chip.

User-programmable options allow "no-glue" interfacing with 8051, 8096, and 80188 microcontroller families. EPROM and port addresses can be relocated within dual-64K-byte memory planes. The programmable RESET input will conform to various microcontrollers. Its flexible architecture allows applications to use multiple Port Expander chips.

The device's flexibility accommodates several microcontroller architectures. Its default mode is ideal for dual-memory-plane 8051 applications. A single plane option conforms to 80188, 68xx, and 8-bit-mode 8096 architectures. The memory-plane overlap option allows address-constrained systems and 8051 systems that have code compiled from high-level languages to use multiple Port Expanders.

*CHMOS is a patented process of Intel Corporation.

October 1989
Order Number: 290165-004

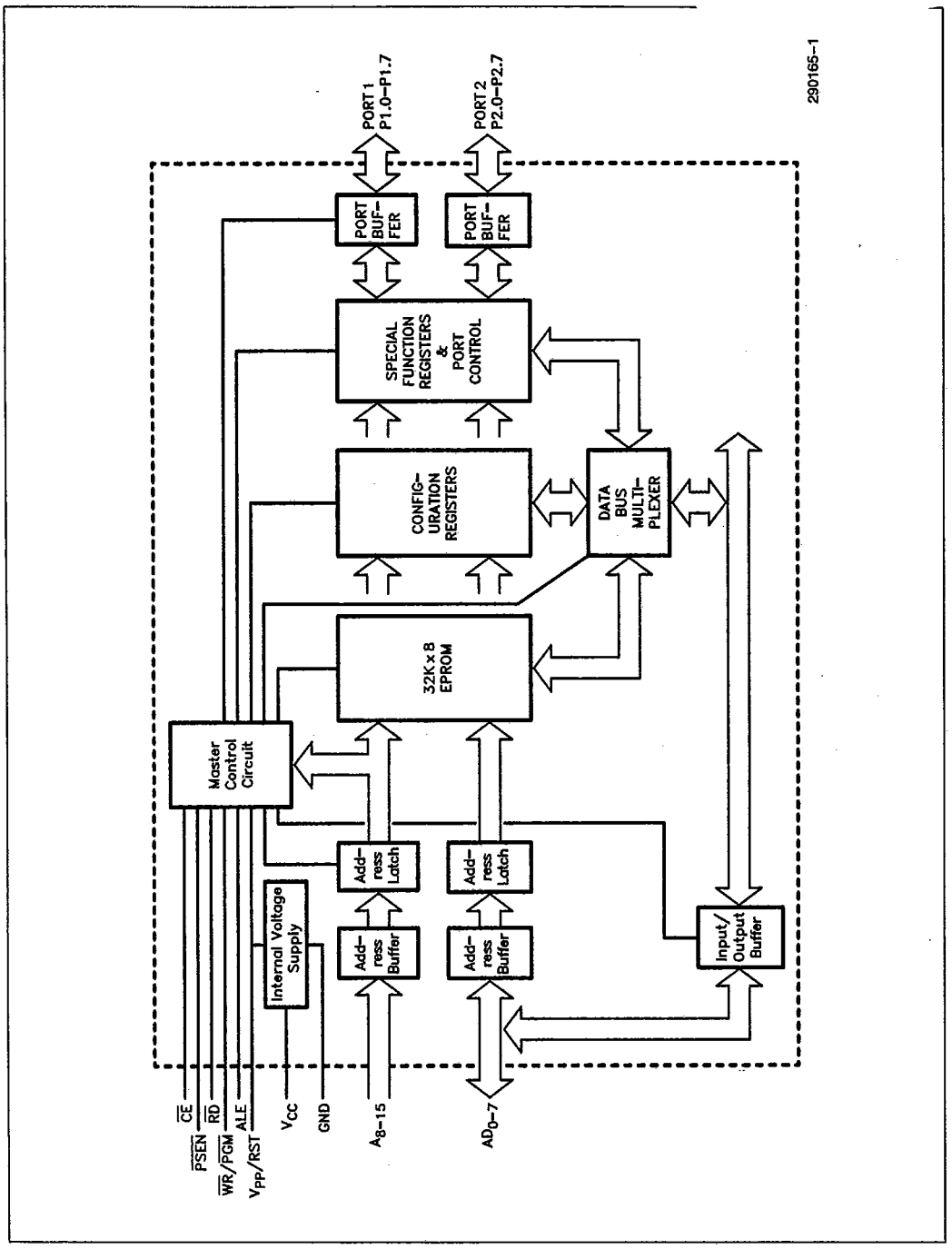


Figure 1. Block Diagram

ARCHITECTURE

Intel's 8051-family and the 87C75PF form the most versatile, integrated microcontroller combination in the industry. No other solution provides a microcontroller, 32K-bytes of EPROM and port expansion in only two chips. Also, the 87C75PF takes full advantage of the 8051's separate program- and data-memory planes. The 87C75PF uses all sixteen address/data lines and all of the 8051's control signals to access two 64K-byte memory planes. In fact, this architecture accommodates two 87C75PFs — 64K-bytes of EPROM and 4 ports — still leaving room for 60K of RAM and other features.

The 87C75PF's versatility makes possible minimum-chip solutions for other microcontroller architectures, too. Single memory-plane modes are user programmable for no-glue interfaces to 8096BH, 80C196, 8098, and 80188 controllers.

Flexible Memory Map

Programmable memory map options will customize the 87C75PF for any application. Intel's 8051 and 8096 microcontrollers have boot-up locations in the lower half of their memory maps. The 87C75PF's EPROM defaults to low memory for these controllers. 80188, 68xx, and 63xx microcontrollers use high-memory boot-up (code and vector) addresses. A user programmable option will move the 87C75PF's EPROM to the device's high-memory addresses. Special Function Registers and port addresses can also be moved to any 2K-byte address boundary.

Programmable Control

Reset level varies depending on the microcontroller family. The 87C75PF's reset (RST) is active-high to match the 8051. Other microcontrollers have active-low reset. A programmable active-low reset option will configure the 87C75PF for these controllers.

Versatile I/O Ports

The 87C75PF has two 8-bit I/O ports. Port 1 is open-drain and port 2 is quasi-bi-directional. The open-drain port can be used for high impedance inputs or "wire-ORed" input/outputs. The quasi-bi-directional port can be used as inputs with built-in pull-up resistors or as low-current-drive outputs. Alternate modes allow either port to have active pull-up (CMOS) outputs. This output mode provides higher current, faster switching, and low power port drive.

Minimum Chip Microcontroller Solution

Primary applications are: 1) single-chip microcontroller systems that have outgrown the controller's internal code-memory and 2) multiple-chip systems that need features-integration, such as redesigned applications that recover ports with discrete components. Typical memory expansion requires EPROM, port expander chips, address latches, address decoder and glue-logic chips — all are incorporated in the 87C75PF (Figure 1).

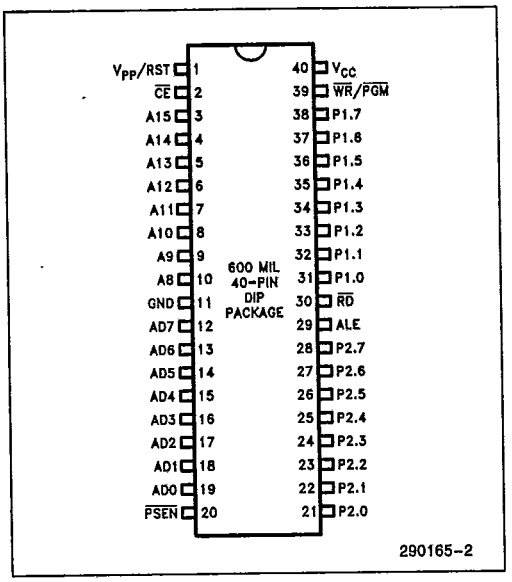


Figure 2. 40-Pin Dip Package

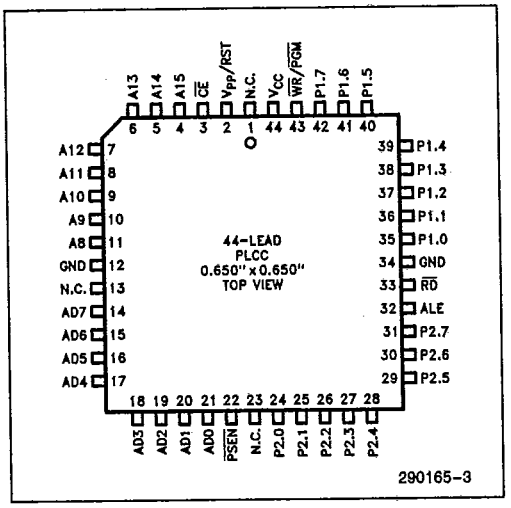


Figure 3. 44-Lead PLCC Package

PIN DESCRIPTIONS

Symbol	Pin Number		Function
	DIP	PLCC	
VPP/RST	1	2	In operating mode, VPP/RST is V_{IL} or V_{IH} and serves as the reset input. RST is user programmable as active-high or active-low via the Control Level Register (CLR.7). When RST is asserted, ports are set to inputs in non-CMOS mode or 1's in CMOS mode. With RST asserted, port-writes have no affect; port-latch-reads return "1s". VPP is the programming supply-voltage input.
$\overline{CE}$	2	3	$\overline{CE}$, the master device enable input, is active-low. When asserted, data can be written and read to/from the device. When $\overline{CE}$ is not asserted, the memory is in standby and cannot be accessed; ports cannot be accessed but maintain their current active states.
A_{15}–A_8	3–10	4–11	High-order addresses flow into the device when ALE = V_{IH} and are latched when ALE = V_{IL}.
GND	11	12,34	VSS (Ground) pins.
AD_7–AD_0	12–19	14–21	Multiplexed low-order address/data. After ALE latches addresses, these pins input or output data depending on $\overline{RD}$, $\overline{WR}/\overline{PGM}$, and $\overline{PSEN}$.
$\overline{PSEN}$	20	22	This active-low pin is the Program Store ENable. EPROM or non-volatile registers are read if this pin is asserted. If bit ELR.6 is programmed ("0"), $\overline{PSEN}$ and $\overline{RD}$ are internally combined. If either or both of these signals is V_{IL}, EPROM or SFR data is accessed depending on the address. When VPP is at its programming voltage, $\overline{PSEN}$ and $\overline{RD}$ are internally combined, as described above. This allows a resident microcontroller to use its $\overline{READ}$ signal to verify programmed data during in-system programming.
P2.0–P2.7	21–28	24–31	8-bit I/O port pins with Quasi-bi-directional (internal pull-up) outputs. All Port 2 pins can be configured as CMOS outputs by programming Control Level Register bit CLR.5.
ALE	29	32	Addresses flow through the latches to address decoders when ALE = V_{IH}. ALE's falling edge latches all addresses independent of $\overline{CE}$. $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}/\overline{PGM}$ are non-functional when ALE is V_{IH}. Read and write modes are possible only when ALE is V_{IL}.
$\overline{RD}$	30	33	During normal operation, $\overline{RD}$ is used to read information from the SFRs. If bit ELR.6 = "0", $\overline{RD}$ and $\overline{PSEN}$ are internally combined (see $\overline{PSEN}$ pin description). During programming, $\overline{RD}$ and $\overline{PSEN}$ are internally combined when VPP is at its programming voltage. This pin's location is the same as a megabit EPROM's GND pin. For compatibility with PROM programmers that force this pin to ground, $\overline{RD}$ becomes non-functional when P1.0 is at V_H.
P1.0–P1.7	31–38	35–42	General purpose 8-bit open-drain I/O port pins. When P1.0 is at V_H (12V) the Configuration Plane can be accessed (see the Mode table) and $\overline{RD}$ is internally disabled. To prevent device damage, Port 1 must be reset, by RST, or have a "1" written to P1.0 before V_H is applied to P1.0. All Port 1 pins can be configured as CMOS outputs by programming Control Level Register CLR.6.
$\overline{WR}/\overline{PGM}$	39	43	The active-low $\overline{WR}/\overline{PGM}$ is used to write data to the SFRs. During programming (VPP = 12.75V), the SFRs cannot be written, and this signal becomes the program-pulse control input.
VCC	40	44	This pin is the supply voltage input.

EXTENDED TEMPERATURE (EXPRESS) uC PERIPHERAL

Intel's EXPRESS microcontroller and application-specific peripheral families receive additional processing to enhance product characteristics. EXPRESS processing is available for several microcontrollers, EPROMs, and peripheral products allowing the appropriate device to match custom system applications. EXPRESS devices are available with 168 ±8 hour, 125°C dynamic burn-in using Intel's standard bias configuration. This process meets or exceeds most industry burn-in specifications. The standard EXPRESS operating temperature range is 0°C to +70°C. EXPRESS extended operating temperature range (−40°C to +85°C) and automotive temperature range (−40°C to +125°C) products are also available. Like all Intel products, the EXPRESS family is inspected to 0.1% electrical AQL. This allows reduction or elimination of incoming testing.

EXPRESS PRODUCT FAMILY

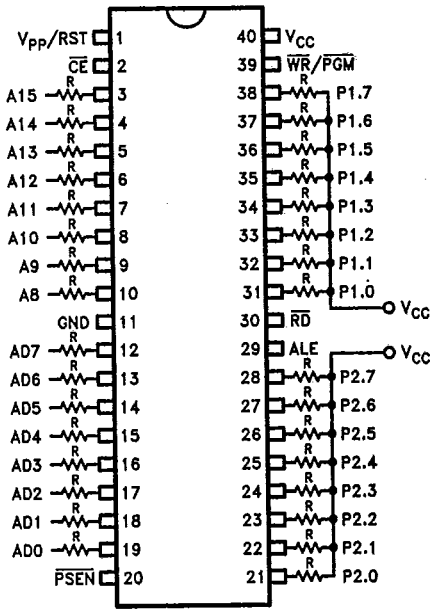
PRODUCT DEFINITIONS

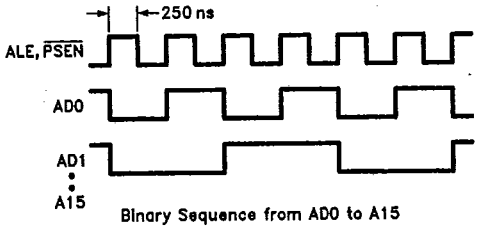
Type	Operating Temperature (°C)	Burn-in 125°C (hr)
Q	0°C to +70°C	168 ±8
T	−40°C to +85°C	NONE
L	−40°C to +85°C	168 ±8

EXPRESS OPTIONS

Speed Versions	Packaging Options	
	CERDIP	PLCC
	Contact your local Intel Sales Office for EXPRESS product availability	

Burn-In Bias and Timing Diagrams





Binary Sequence from AD0 to A15

This cycle also includes port read/write accesses.

V_{CC} = +5V, V_{PP}/RST = +5V, $\overline{CE}$ = GND, $\overline{RD}$ = +5V, $\overline{WR}/\overline{PGM}$ = +5V, R = 10K

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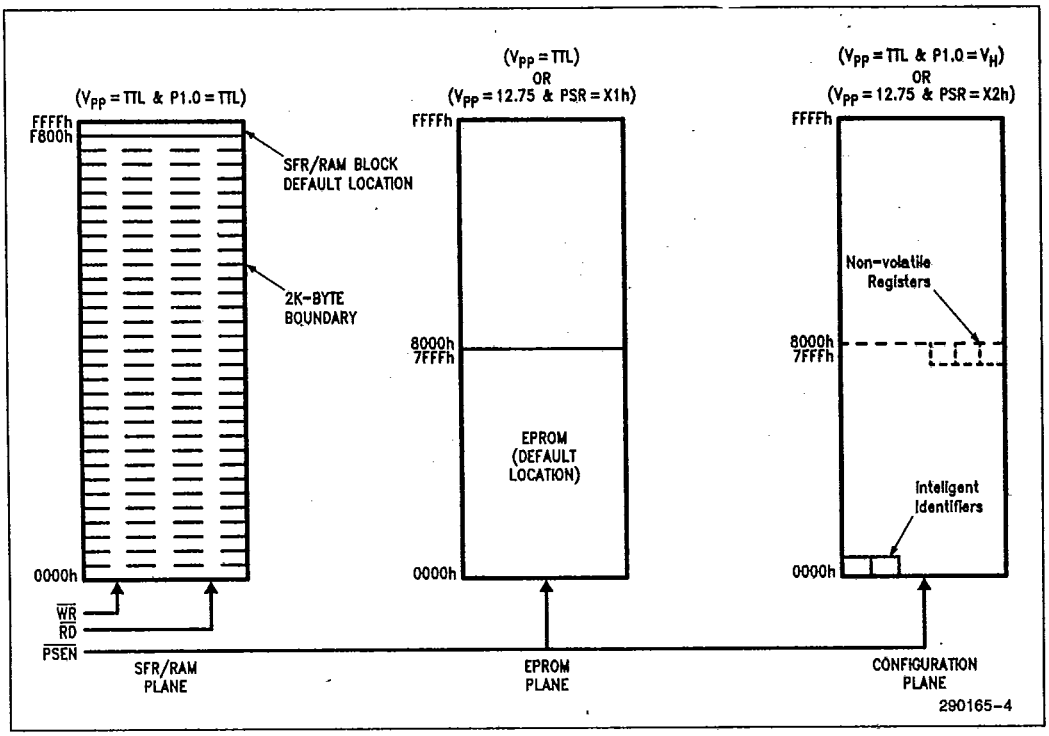


Figure 4. The Port Expander's 3-Plane Memory Map

MEMORY MAP

The Port Expander contains three memory planes — EPROM plane, special function register/RAM (or SFR/RAM) plane, and the configuration plane. Figure 4 shows the three memory planes.

The EPROM's default location (in an erased device) is at the bottom 32K bytes (0000h to 7FFFh) of the 64K-byte EPROM plane. The default location of the special function register block is F800h to FFFFh in the SFR/RAM plane. Non-volatile registers (NVRs) are mapped at addresses 7FFDh through 7FFFh in the configuration plane.

Non-volatile registers are used to program the locations of the EPROM, SFR block, and other features (see Figure 7). In normal operating mode, the configuration plane cannot be accessed; only the EPROM and SFR/RAM planes are available. During programming/verification, the plane select register, PSR, (SFR default location F810h) determines which plane — EPROM or configuration — is accessed. The EPROM array is programmed/verified if PSR contains xxxxxx01b (X1h). The configuration plane is programmed/verified if PSR contains xxxxxx10b (X2h) before V_{PP} is raised to 12.75V.

NVRs in the configuration plane are also read if pin P1.0 = V_H (12V) while V_{PP} = TTL. This allows PROM programmers to identify the device, download its configuration, and program duplicates accordingly.

ARCHITECTURE FLEXIBILITY

The Port Expander can operate in several configurations. The configuration plane's non-volatile registers configure the device for microcontroller-architecture compatibility.

8051 architecture accommodates two 64K-byte memory planes — program-memory and data-memory planes. In its default mode (erased) the device is configured with these two independently addressable planes — a perfect companion for the 8051 family.

Many other 8-bit microcontrollers (8096BH, 8098, Z8xx, 68xx, etc.), and 8051s with code compiled from high-level languages, can handle only one 64K-byte memory plane. Another mode configures the device for single plane operation — again, a perfect 8-bit microcontroller companion device.

Often, more than two external ports and greater than 32K-bytes of external EPROM are required in single-memory-plane applications. Another mode allows two Port Expanders to supply 60K-bytes of EPROM and four 8-bit I/O ports — still leaving 4K-bytes for other read/write devices.

Double-plane Applications

The default configuration has two memory planes; program (EPROM) and data (SFR/RAM). This configuration is consistent with the 8051 architecture. The EPROM plane is read-only and is accessed by $\overline{PSEN}$. The SFR/RAM plane is a read/write plane that is accessed by the $\overline{RD}$ and $\overline{WR}/\overline{PGM}$ inputs. These signals and the sixteen address inputs provide two 64K-byte memory-planes.

Single-plane Applications

Many microcontroller architectures have only one 64K-byte memory plane. One way to configure the device for a single-plane is to simply tie $\overline{PSEN}$ and $\overline{RD}$ together and connect the combined read signal to the system's $\overline{READ}$ line.

8051 machine code compiled from high-level languages often can't deal with separate program- and data-planes. Systems using high-level languages usually form one 64K-byte memory plane by combining $\overline{PSEN}$ and $\overline{RD}$ into a common $\overline{READ}$ signal (by using an AND gate).

The Port Expander provides a better solution. If the EPROM Location Register bit ELR.6 is programmed, $\overline{PSEN}$ and $\overline{RD}$ are combined internally to form a common $\overline{READ}$ signal. Either of these signals can be used to gate data from the EPROM plane and/or SFR/RAM plane to the outputs. In effect, this mode forms a single 64K-byte memory plane. For 8051 high-level-language systems, no external glue is required to "AND" $\overline{PSEN}$ with $\overline{RD}$. The 8051's $\overline{PSEN}$ and $\overline{RD}$ signals can be connected directly to the Port Expander's corresponding inputs. Single-plane, non-8051 microcontroller systems need to route their $\overline{READ}$ line to either, or both, $\overline{PSEN}$ or $\overline{RD}$. If only one input is used, the other must be tied high.

Overlapped Single Plane

Two Port Expanders can fit in a single-memory-plane system by programming the configuration plane's non-volatile registers. To accomplish this, each device must have its SFR block mapped over a portion of its EPROM array. The SFR block can be placed on any 2K-byte boundary by programming the SFRLR. EPROM Location Register bit ELR.7 allows the EPROM to be moved to high memory or to remain in its default low-memory location. Programming ELR.6, the overlap bit, allows the EPROM plane to be mapped over the SFR/RAM plane; this also internally combines $\overline{PSEN}$ and $\overline{RD}$. 2K EPROM bytes located at the SFR block's base-address are disabled and replaced by the 2K-byte SFR block.

Figure 5 shows various memory configurations.

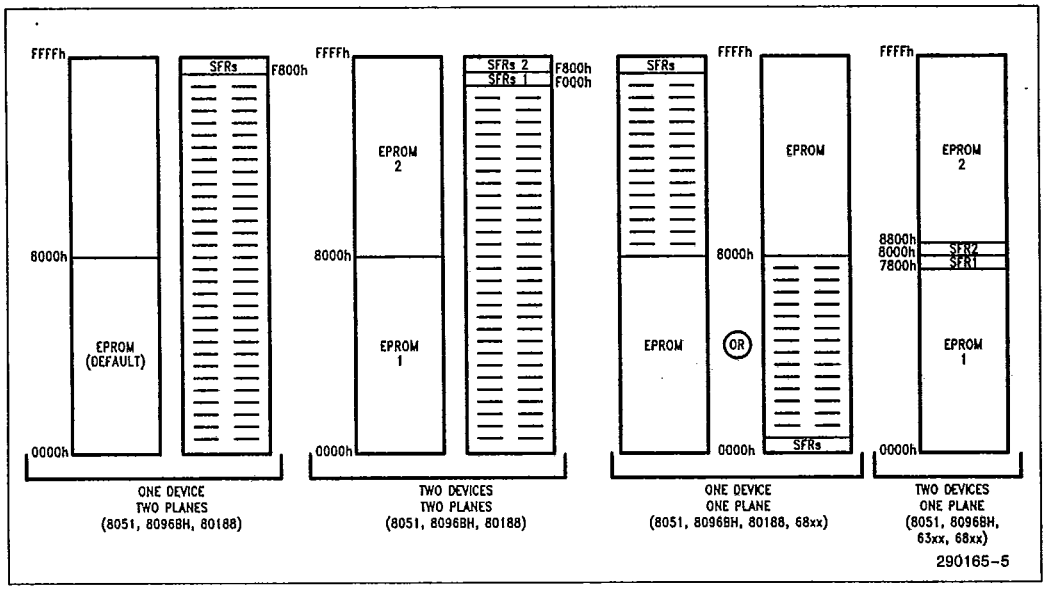


Figure 5. A Few Possible Memory Plane Configurations

EPROM

The Port Expander contains a 32,768 x 8-bit EPROM. When erased, the EPROM is located between EPROM plane addresses 0000h and 7FFFh. This is a common boot-up address range for most microcontrollers, including 8051 and 8096 families. For microcontrollers that reset in high addresses, the EPROM can be relocated to device addresses 8000h through FFFFh via the EPROM Location Register. This also allows systems to use two Port Expanders — one with EPROM at low-memory and the other with EPROM relocated at high-memory.

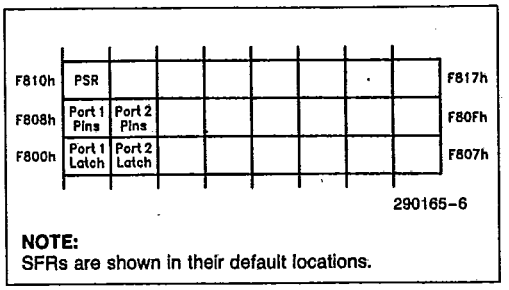
When a valid address is present, $\overline{PSEN}$ controls EPROM access. Asserting $\overline{PSEN}$ during non-valid addresses places device outputs at high impedance.

SPECIAL FUNCTION REGISTERS (SFRs)

SFR addresses described below and in Figure 6 are default in an erased device. A 2K-byte block (default locations F800h through FFFFh) is reserved for ports, plane select register (PSR), and future features. The SFR/RAM-block base address can change depending on the SFRLR's five most-significant bits (Figure 10). Only five SFR/RAM-block locations are defined. Accessing any other addresses in this block places the external bus in a high impedance state allowing external devices to occupy these locations.

Ports are accessed by reading or writing the SFRs. Port 1 and Port 2 latch data is read/written by accessing locations F800h and F801h. F802h through F807h are reserved for future port latches. Port 1 and Port 2 pins are read at F808h and F809h. Writing to these locations has no effect. F80Ah through F80Fh are reserved for future port-pin locations.

F810h is a two-bit read/write plane select register (PSR). During program/verify, PSR's value before V_{PP} = 12.75V determines whether the EPROM- or configuration-plane is accessed. If PSR contains xxxxxx01b, the EPROM plane is programmed and verified. If PSR contains xxxxxx10b, configuration plane registers will be programmed and verified. In operating mode, the configuration plane cannot be accessed. However, in the configuration read mode (P1.0 = V_H and V_{PP} = TTL) configuration registers can be read (only) and the SFRs can be written (only).



NOTE:
SFRs are shown in their default locations.

Figure 6. SFR Memory Map

CONFIGURATION PLANE

Non-Volatile Registers (NVRs)

The configuration plane contains the inteligent Identifier™ and non-volatile registers. This plane is read:

1) if P1.0 = V_H (V_H = 12V ±1V) while V_{PP} = TTL
   or
2) if PSR contains xxxxxx10b while V_{PP} = 12.75V.

Inteligent Identifier codes are at 0000h (manufacturer) and 0001h (device). NVRs are at 7FFDh (CLR), 7FFEh (ELR), and 7FFFh (SFRLR).

NVRs are programmed/verified by writing xxxxxx10b to PSR before V_{PP} = 12.75V; inteligent Identifier bytes are read-only. Figure 7 shows the configuration plane's NVR locations. Condition 1) above allows PROM programmers to check the device's configuration and locate the SFRs and EPROM. NVRs are EPROM cells which, when erased, contain "1s".

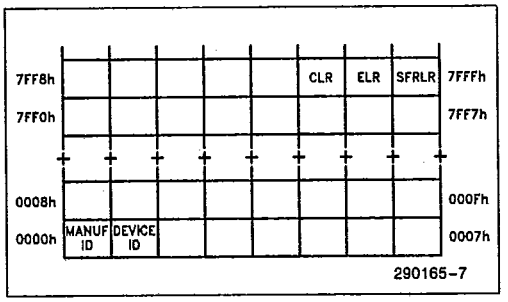


Figure 7. Configuration Plane Memory Map

Control Level Register (CLR)

The Control Level Register, CLR (7FFDh), is used to change the RST pin's active level and port output drive. RST is active-high and CMOS port-drive is disabled in an erased device. If the reset level bit, RSTL (CLR.7), is programmed ("0"), RST is active-low. Port 1 and/or Port 2 outputs will be CMOS if P1C (CLR.6) and/or P2C (CLR.5) are programmed.

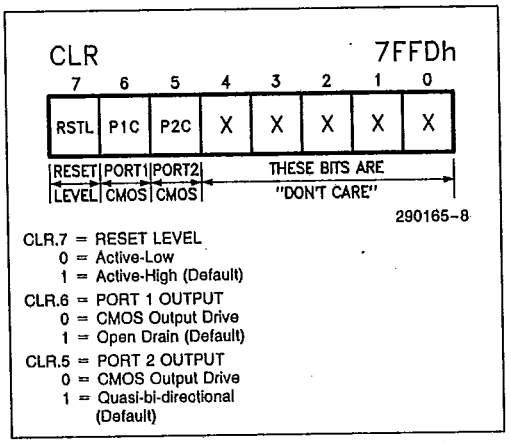


Figure 8. Control Level Register (CLR)

EPROM Location Register (ELR)

The EPROM Location Register (ELR) is at 7FFEh. The EPROM location bit, EL (ELR.7), places the EPROM at either top or bottom EPROM-plane addresses. When erased, the EPROM array is at 0000h–7FFFh in the 64K-byte address space. Programming ELR.7="0" places the EPROM at 8000h–FFFFh.

When erased, the overlap option is disabled. EPROM and SFR/RAM blocks are in default locations. $\overline{PSEN}$ accesses EPROM- and $\overline{RD}$ accesses the SFR-data.

If the OVERLAP bit, OVLP (ELR.6), is programmed, EPROM and SFR/RAM planes overlap. $\overline{PSEN}$ and $\overline{RD}$ are internally combined. If either is V_{IL}, EPROM or SFR data is accessed depending on the address.

If the SFR/RAM block's 2K-byte boundary overlaps the EPROM array and ELR.6=0, the SFR/RAM block replaces 2K EPROM bytes. Accessing non-defined bytes in the 2K-byte space places the external bus in a high-Z state. By programming ELR.6, one-memory-plane microcontrollers (8096, 80188, 68xx) and 8051s with high-level-language-compiled code can use two 87C75PFs.

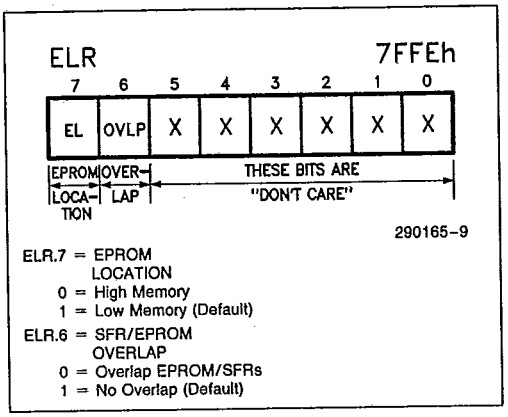


Figure 9. EPROM Location Register (ELR)

SFR Location Register (SFRLR)

The SFRLR (7FFFh) determines the SFR/RAM block's five most-significant base-address bits; SFRLR.7 = A15, SFRLR.6 = A14, SFRLR.5 = A13, SFRLR.4 = A12, and SFRLR.3 = A11. Programming this register places the SFR/RAM block on any 2K-byte boundary. For example, the SFRs are placed at 2800h by programming 00101xxxb.

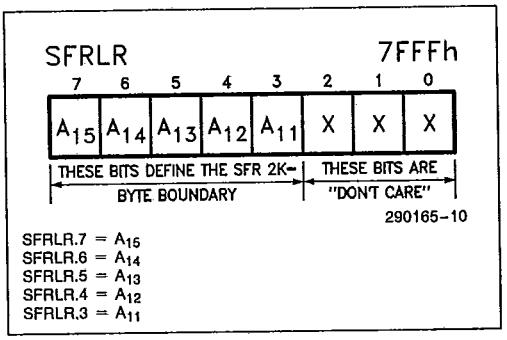


Figure 10. SFR Location Register (SFRLR)

Port 1

Port 1 has 8 open-drain, bi-directional pins. Pins float if "1s" are written to latches or RST is asserted. They can then serve as high impedance inputs.

P1.0 receives high voltage (V_H = 12V) during the inteligent Identifier/NVR Mode. P1.0 MUST BE RESET (BY RST OR BY WRITING "1" TO P1.0) BEFORE APPLYING V_H. For megabit PROM programmer compatibility, P1.0 = V_H disables $\overline{RD}$.

All Port 1 pins are CMOS outputs (TTL level in 200ns, CMOS level in 1us) if P1C is programmed (CLR6="0"). Asserting RST or writing "1s" will present CMOS V_{OH} levels. CMOS-configured Port 1 pins should not be used as inputs. Port latch writes occur on $\overline{WR}$'s rising edge to prevent glitches when changing individual bits; other bits are not affected.

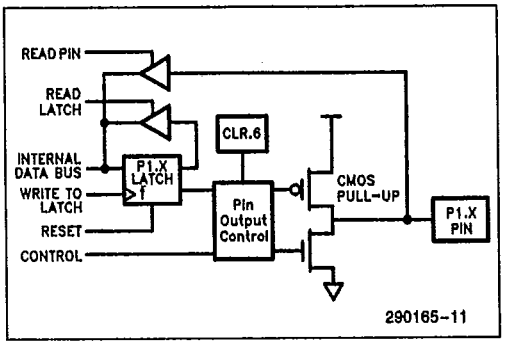


Figure 11. Port 1 Pin Diagram

Port 2

Port 2 is an 8-bit quasi-bi-directional port. Writing "1s" asserts short-duration active pull-ups to guarantee TTL V_{OH} levels within 200ns. Port 2 pins are held high by internal pull-ups allowing them to serve as inputs. Pins pulled low externally source current (I_{IL}). Port 2 latches are set to "1s" upon reset.

Programming P2C (CLR.5="0") configures Port 2 as CMOS outputs. Asserting RST or writing "1s" outputs CMOS V_{OH} levels. CMOS-configured Port 2 pins should not be used as inputs. Port latch writes occur on $\overline{WR}$'s rising edge to prevent glitches when changing individual port bits; other bits are not affected.

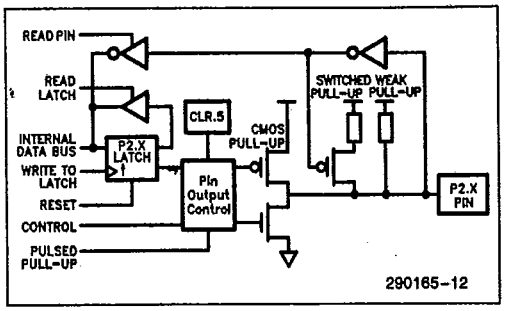


Figure 12. Port 2 Pin Diagram

SYSTEM APPLICATIONS

The 87C75PF significantly reduces chip count and interfacing hardware in multiplexed address/data bus systems. Figure 13 shows a low power, small board space, minimum chip design. The controller's multiplexed bus (AD_{0-7}) is tied to the 87C75PF's address/data pins. Separate address latches and address decoders are not needed because the 87C75PF latches all sixteen addresses and decodes internal features within its two 64K-byte memory planes.

ALE controls the 87C75PF's internal address latches. A V_{IH} to V_{IL} transition latches the present address. $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ control data-flow between the controller and 87C75PF. 8051, 8096, and 80188 families benefit from the 87C75PF's "no-glue" interface.

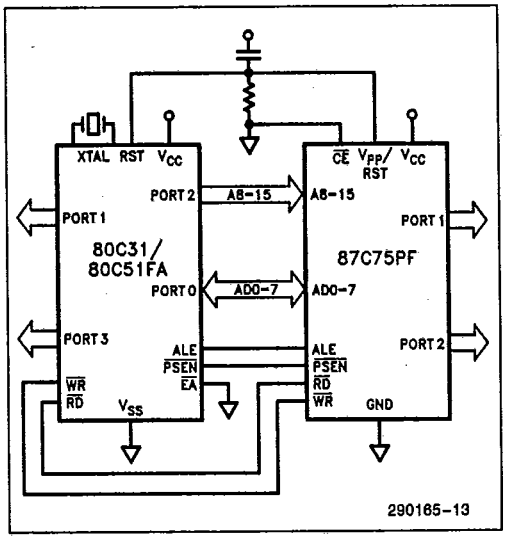


Figure 13. "No-glue" 80C51 with 87C75PF

Table 1. MODE SELECTION 87C75PF (default configuration shown)

MODE	$\overline{CE}$	$\overline{PSEN}$	$\overline{RD}$	$\overline{WR}/\overline{PGM}$	ALE(6)	V_{PP}/RST(4)	V_{CC}	P1.0(2)	AD_{0-7}
Reset	X(1)	X	X	X	X	V_{IH}	5V	X(10)	X
Read EPROM(12)	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	5V	X	D Out
Read SFR(12)	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	5V	X	D Out
Single Plane Read(8)	V_{IL}	V_{IL} or V_{IL}		V_{IH}	V_{IL}	X	5V	X	D Out
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IL}	X	5V	X	High Z
Write SFR	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}(14)	5V	X or V_H	D In
Write Disable	V_{IL}	X	X	V_{IH}	V_{IL}	X	5V	X	High Z
Read/Write Disable	V_{IL}	X	X	X	V_{IH}	X	5V	X	High Z
Standby	V_{IH}	X	X	X	X	X	5V	X	High Z
Program EPROM/NVR(5)	V_{IL}	V_{IH}	X(11)	V_{IL}	V_{IL}	V_{PP}(3)	V_{CP}(3)	V_H(7)	D In
EPROM/NVR Verify(5)	V_{IL}	V_{IL}	X(11)	V_{IH}	V_{IL}	V_{PP}	V_{CP}	V_H	D Out
Program Inhibit	V_{IH}	X	X	X	X	V_{PP}	V_{CP}	X	High Z
Alternate Program	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{PP}	V_{CP}	X	D In
Alternate Verify(9)	V_{IL}	V_{IL} or V_{IL}		V_{IH}	V_{IL}	V_{PP}	V_{CP}	X	D Out
NVR Config Read(13)	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	X(7)	5V	V_H	D Out
inteligent(13) Identifier - Manuf	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	X(7)	5V	V_H	89h
inteligent(13) Identifier - Device	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	X(7)	5V	V_H	D0h

NOTES:
1. X can be V_{IL} or V_{IH}.
2. $V_H = 12.0V \pm 1V$.
3. $V_{PP} = 12.75V$ and $V_{CP} = 6.25v$ during programming.
4. RST is active-high (erase default shown) or programmable via CLR.7 as active-low.
5. The EPROM array is programmed/verified if PSR = X1h. The NVR array is programmed/verified if PSR = X2h. NVRs and inteligent Identifier can be read when P1.0 = V_H and V_{PP} = TTL.
6. Data cannot be read/written when ALE = V_{IH}. ALE must toggle — V_{IH} to V_{IL} — to latch addresses.
7. Reset must occur via V_{PP}/RST or "1" written to P1.0 before P1.0 = V_H.
8. If ELR.6 = 0, $\overline{PSEN}$ and $\overline{RD}$ are internally combined.
9. If $V_{PP} = 12.75V$, $\overline{PSEN}$ and $\overline{RD}$ are internally combined. If either is V_{IL}, EPROM (PSR = X1h) or NVR (PSR = X2h) data is verified. If P1.0 = V_H, $\overline{RD}$ is non-functional. If V_{PP} = TTL and P1.0 = V_H, only NVRs and inteligent Identifier can be read.
10. RST sets port latches to "1s". After reset, P1.0 (= "1") is protected when V_H is applied.
11. For programmer compatibility, the 87C75PF's $\overline{RD}$ is disabled when P1.0 = V_H.
12. $\overline{PSEN}$ and $\overline{RD}$ can be asserted simultaneously unless the EPROM and SFRs overlap & ELR.6 = 1.
13. Addresses must be latched during Identifier/NVR reads.
14. RST not asserted.

DEVICE OPERATION

Table 1 lists 87C75PF operating and programming modes. Operating modes require a 5V power supply. Programming modes require 12.75V V_{PP}, 6.25V V_{CC}, and 12.0V Identifier/NVR-read voltages. All input levels are TTL or CMOS except V_{PP}, V_{CP}, and V_H.

OPERATING MODES

Reset

RST is an active-high input in an erased device. Programming CLR.7 ("0") makes RST active-low. Asserting RST for 500ns sets port latches to "1s". RST affects no other writable locations. Before a PROM programmer enters the inteligent Identifier/NVR read mode, RST should be asserted (or "1" written to P1.0) to set P1.0's pin. This protects P1.0 from damage by the 12.0V identifier voltage.

EPROM Read Mode

$\overline{PSEN}$ enables EPROM data onto AD_{0-7} and controls the device's output buffer. This active-low pin functions only when $\overline{CE}$ and ALE are asserted. When an address is latched (ALE = V_{IL}), access time (t_{AVDV}) equals the $\overline{CE}$ to output delay (t_{CLDV}). Outputs display valid data t_{ELDV} after $\overline{PSEN}$'s falling edge, assuming t_{AVDV} and t_{CLDV} times are met.

SFR Read Mode

$\overline{RD}$ enables SFR data onto AD_{0-7} and controls the device's output buffer. This active-low pin functions only when $\overline{CE}$ and ALE are V_{IL}. EPROM read mode timing requirements apply to this mode.

Single Plane Read Mode

This mode allows single-plane microcontrollers and 8051-family controllers with older-version high-level-language-compiled code to use an 87C75PF without "glue" devices. It is possible to assert $\overline{PSEN}$ and $\overline{RD}$ simultaneously. Data bus conflict will not occur if the SFRs are not memory mapped over EPROM array addresses. If SFR and EPROM addresses overlap, bus conflict can be avoided if the EPROM location register's "Overlap" bit (ELR.6) is programmed. Programming this bit also internally combines $\overline{PSEN}$ and $\overline{RD}$. Asserting either (or both) enables EPROM or SFR data, depending on the address, onto AD_{0-7}. See the "Overlapped Single Plane" section for details.

Output Disable Mode

If $\overline{PSEN}$ and $\overline{RD}$ are not asserted, the device's output buffers (AD_{0-7}) are disabled. Data can be written to the 87C75PF or transferred to/from other devices.

SFR Write Mode

$\overline{WR}/\overline{PGM}$ enables data on AD_{0-7} to be written into the SFRs. This active-low pin functions only when $\overline{CE}$ and ALE are V_{IL}. When an address is latched (ALE = V_{IL}) and data has been present for t_{DVWH}, $\overline{WR}$'s rising edge latches data into an SFR. Other A.C. timing parameters must be observed.

Write Disable

SFR data cannot be written when $\overline{WR}/\overline{PGM}$ is high. Low-address and data share common pins, but the device allows new addresses only when ALE is high; data can be written only when ALE is low.

Read/Write Disable

Since the Port Expander uses a multiplexed address/data bus, data can be read or written only if a valid address is latched. To prevent erroneous reads or spurious writes of invalid data, $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}/\overline{PGM}$ are non-functional when ALE is high; however, new address information can enter the address latches. ALE's falling edge latches the address and enables $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}/\overline{PGM}$.

Standby Mode

Standby mode substantially reduces V_{CC} current. $\overline{CE}$ = V_{IH} places output buffers in low-power, high impedance mode independent of $\overline{PSEN}$, $\overline{RD}$, or $\overline{WR}$. Two-line output control ($\overline{CE}+\overline{PSEN}$ or $\overline{CE}+\overline{RD}$) provides:

a) minimum memory power dissipation, and

b) assurance that data bus contention will not occur.

To efficiently use two-line control, address decoding circuitry should enable $\overline{CE}$. $\overline{PSEN}$ should be connected to the microcontroller's program-store enable ($\overline{PSEN}$), $\overline{RD}$ to the controller's data-read enable ($\overline{RD}$), and $\overline{WR}/\overline{PGM}$ to its write control ($\overline{WR}$). This assures that only selected memory and peripheral devices have active inputs and outputs while non-selected devices are in low-power standby mode.

PROGRAMMING MODES

EPROM/Configuration (NVR) Programming Mode

Initially and after each erasure, all EPROM and NVR bits are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" are programmed, the data word can contain both "1s" and "0s". Ultraviolet light erasure is the only way to change "0s" to "1s".

The programming mode is entered when V_{PP} is raised to its programming voltage. After latching an address, data is programmed by applying an 8-bit word to data pins AD_{0-7}. Pulsing $\overline{WR}/\overline{PGM}$ to TTL-low while $\overline{CE}$ and ALE are V_{IL} will program data. TTL levels are required for address and data inputs.

To accommodate PROM programmers that force the $\overline{RD}$ pin to ground (DIP pin 30), applying 12V to port pin P1.0 will internally disable the 87C75PF's $\overline{RD}$ input. When V_{PP} is not at its programming voltage the device is in the inteligent Identifier mode. When V_{PP} is raised for programming, the inteligent Identifier mode is disabled.

EPROM and NVR Verify

With V_{PP} and V_{CC} at their programming levels and $\overline{CE}$ asserted, EPROM or configuration data (depending on PSR's contents) can be verified. To simplify on-board and in-system programming, $\overline{PSEN}$ and $\overline{RD}$ are internally combined when V_{PP} is at its programming level. Either signal can be used to verify programmed data (if P1.0 is not V_H).

For compatibility with PROM programmers equipped for word-wide megabit EPROMs, DIP-pin 30 — the 87C75PF's $\overline{RD}$ pin — is internally disabled when P1.0 is V_H.

Program Inhibit

The Program Inhibit mode allows parallel programming and verification of multiple devices with different data. With V_{PP} at its programming voltage, a $\overline{WE}/\overline{PGM}$ pulse programs any device that has $\overline{CE}$ asserted. Programming is inhibited on any device with $\overline{CE}$ not asserted.

Alternate Programming and Verification Modes

For programmers that can apply V_{IH} or V_{CC} to $\overline{RD}$, the EPROM and NVRs can be programmed using a more conventional slow-motion write-mode-type algorithm. 12V need not be applied to P1.0 to disable the $\overline{RD}$ pin during the alternate programming mode. $\overline{PSEN}$ and $\overline{RD}$ are internally combined when V_{PP} is applied, and either signal can be used to enable EPROM or NVR data during program verification. See the Quick-Pulse Programming algorithm flowchart and waveforms at the end of this data sheet.

inteligent Identifier™/NVR Mode

Programming equipment determines the device's manufacturer, type, and configuration (NVR contents) by using the inteligent Identifier/NVR Mode. A programmer can read a master device's identifier and NVRs, select the proper algorithm, and program duplicates accordingly.

The configuration plane is accessed by raising port pin P1.0 to V_H = 12.0V. Before P1.0 is brought to V_H, Port 1 must be reset by asserting the V_{PP}/RST pin or by writing a "1" to P1.0's latch. When ALE latches a valid address and $\overline{PSEN}$ is V_{IL}, identifier/NVR data appears on Address/Data pins AD_{0-7}. For compatibility with programmers that support megabit EPROMs, $\overline{RD}$, which is usually forced to ground, is "don't-care" when P1.0 = V_H. When $\overline{CE}$, ALE, and $\overline{PSEN}$ are V_{IL} and P1.0 = V_H, identifier/NVR data can be read. While in this mode, the SFR/RAM plane cannot be read but can be written. The PSR register can be configured so that either the EPROM or configuration plane is programmed when V_{PP} is raised. This mode's temperature range is 25°C ±5°C.

The inteligent identifier™ mode is not available when:

1. EPROM Location Register bit ELR.6 is programmed to "0", allowing overlap of EPROM and SFR/RAM blocks, and
2. SFR Location Register bits SFRLR.7-3 are programmed to "0"s, moving the SFR/RAM block to its lowest possible 2K block location.

The SFR overlap at 0000H-07FFH not only overrides EPROM in this range but also disables the manufacturer ID at 0000H and device ID at 0001H. However, overlap of the SFR/RAM block at 7800-7FFFH **does not** override NVR reads at locations 7FFDH (CLR), 7FFEH (ELR) and 7FFFH (SFRLR).

ABSOLUTE MAXIMUM RATINGS*

Read Operating Temperature.....0°C to +70°C(2)
Case Temperature Under Bias..−10°C to +80°C(2)
Storage Temperature .....−65°C to +150°C
All Input or Output Voltages.....−2.0V to +7.0V(1)
with Respect to Ground
Voltage on Pin P1.0 .....−2.0V to +13.5V(1)
with Respect to Ground
V_{PP} Supply Voltage.....−2.0V to +14.0V(1)
with Respect to Ground
V_{CC} Supply Voltage .....:...+2.0V to +7.0V(1)
with Respect to Ground

Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTICE: Specifications contained within the following tables are subject to change.

READ/WRITE BUS OPERATION

D.C. CHARACTERISTICS TTL and NMOS Inputs; see A.C. Characteristics for V_{CC} versions offered

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Load Current (A_{8-15})			1.0	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current (AD_{0-7})			10	μA	V_{OUT} = 0V to V_{CC}
I_{SB}	V_{CC} Current Standby	6		5	mA	$\overline{CE}$- inactive, ALE = V_{IL}
I_{CC}	V_{CC} Current Active	4		60	mA	$\overline{CE}$-active, ALE = V_{IH} f(Hz) = 5 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage	1	−0.5	0.8	V	
V_{IH}	Input High Voltage		2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	1	2.4		V	I_{OH} = −400 μA
I_{OS}	Output Short Circuit Current	5		100	mA	

D.C. CHARACTERISTICS CMOS Inputs; See A.C. Characteristics for V_{CC} versions offered.

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Load Current (A_{8-15})			1.0	μA	V_{IN} = 0V to V_{CC}
I_{LO}	Output Leakage Current (AD_{0-7})			10	μA	V_{OUT} = 0V to V_{CC}
I_{SB}	V_{CC} Current Standby	3, 6		5	mA	$\overline{CE}$-inactive, ALE = V_{IL}
I_{CC}	V_{CC} Current Active	3 4		45	mA	$\overline{CE}$-active, ALE = V_{IH} f(Hz) = 5 MHz, I_{OUT} = 0 mA
V_{IL}	Input Low Voltage	1	−0.2	0.8	V	
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC}+0.2	V	
V_{OL}	Output Low Voltage			0.40	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	1	V_{CC}−0.8		V	I_{OH} = −400 μA
I_{OS}	Output Short Circuit Current	5		100	mA	

NOTES:
1. Minimum DC input voltage is −0.5V during transitions. Inputs may undershoot to −2.0V for periods less than 20 ns. Maximum output-pin DC voltage is V_{CC}+0.5V; overshoot may be V_{CC}+2.0V for periods less than 20 ns.
2. This specification defines commercial-product operating temperatures. EXPRESS and Automotive versions are available as noted.
3. $\overline{CE}$ is V_{CC} ±0.2V (87C75PF inactive) or ±0.2V (87C75PF active). Other inputs can have any value within specification.
4. Maximum current value with outputs unloaded.
5. One output shorted for no more than one second. I_{OS} is sampled but not 100% tested.
6. Port latches set to "1s"; outputs unloaded.

PORTS/RESET

D.C. CHARACTERISTICS See A.C. Characteristics for V_{CC} versions offered.

Symbol	Parameter		Notes	Min	Max	Units	Test Conditions
I_{LI}	Input Leakage Current Port 1 Open Drain		1		10	μA	0.4V ≤ V_{IN} ≤ V_{CC}
I_{IL}	Logic 0 current Port 2 (Quasi-bi-directional)		2		−50	μA	P2.x latch = "1", V_{IN} = 0V
V_{IL}	Input Low Voltage	Ports 1&2		−0.5	0.2 V_{CC}−0.1	V	
		RST Input	3	−0.5	0.2 V_{CC}−0.1	V	
V_{IH}	Input High Voltage	Ports 1&2		0.2 V_{CC}+.9	V_{CC}+0.5	V	
		RST Input	3	0.7 V_{CC}	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage				0.40	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	CMOS mode		2.4		V	I_{OH} = −400 μA
		Ports 1&2		0.9 V_{CC}		V	I_{OH} = −40 μA
		Quasi-bi-dir Port 2		2.4		V	I_{OH} = −60 μA
				0.9 V_{CC}		V	I_{OH} = −10 μA

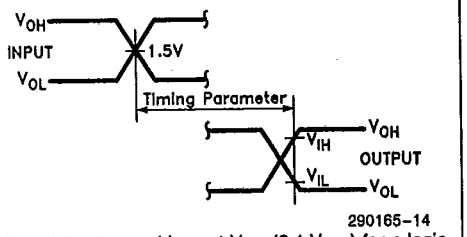
NOTES:
1. Input Leakage current does not apply to Port 2.
2. This specification assumes that Port 2 pins are internally driven to "1" but are externally pulled low
3. RST has hysteresis. V_{IL} is valid at or below 0.2 V_{CC} − 0.1V. V_{IH} is valid at or above 0.7 V_{CC}.

CAPACITANCE(1) T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Max	Units	Conditions
C_{IN}	Address/Control Capacitance	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	12	pF	V_{OUT} = 0V
C_{VPP}	RST/VPP Capacitance	25	pF	V_{IN} = 0V
$C_{I/O}$	Port Pin Capacitance	10	pF	V_{OUT} = 0V

NOTE:
1. Sampled. Not 100% tested.

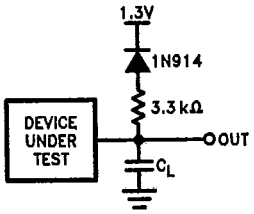
A.C. INPUT/OUTPUT REFERENCE WAVEFORMS



290165-14

A.C. test inputs are driven at V_{OH} (2.4 V_{TTL}) for a logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0".
Input timing begins at 1.5V.
Output timing ends at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}).
Input Rise and Fall Times (10% to 90%) ≤ 10 ns.

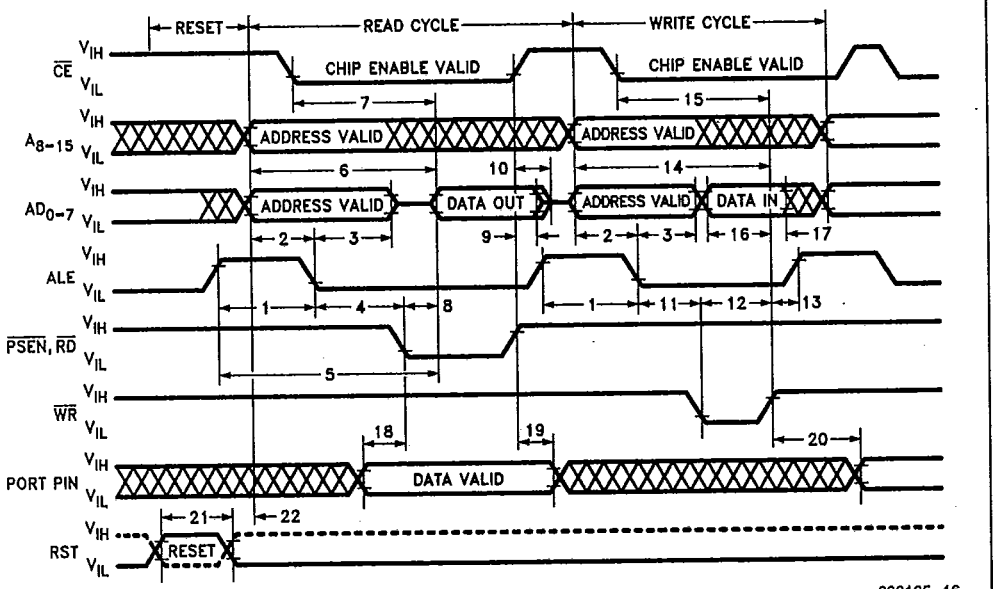
A.C. TESTING LOAD CIRCUIT



290165-15

C_L = 100 pF
C_L Includes Jig Capacitance

READ AND WRITE WAVEFORMS



290165-16

EXPLANATION OF A.C. SYMBOLS

Each timing symbol has five characters. The first is always a "t" (for time). Second and fourth characters represent signal names. Third and fifth represent the signal's logical state. The following list shows character representations.

A: Address
C: Chip Enable or VCC Supply Voltage
D: Data (or instruction)
E: $\overline{PSEN}$ or $\overline{RD}$ Enable
G: $\overline{PGM}$ (Program Strobe)
H: Logic High level
L: ALE or Latch Enable
P: VPP Programming Voltage
Q: Port Output
S: RST (Reset Pin)
T: Time
V: Valid
W: Write Enable
X: No longer a valid "driven" logic level
Z: Float or High-Z level

For example,
t_{AVLL} = Time from Address Valid to ALE Low
t_{LLEL} = Time form ALE Low to Enable ($\overline{PSEN}$ or $\overline{RD}$) Low

A.C. CHARACTERISTICS: READ & WRITE $0°C \leq T_A \leq +70°C$

Parameter		Versions	$V_{CC} \pm 10\%$	87C75PF-200V10		87C75PF-250V10		Unit
No	Symbol	Characteristic	Notes	Min	Max	Min	Max	
1	t_{LHLL}	ALE Pulse Width		50		50		ns
2	t_{AVLL}	Address Valid to ALE Low		7		15		ns
3	t_{LLAX}	Address Hold after ALE Low		20		30		ns
4	t_{LLEL}	ALE Low to $\overline{PSEN}$ or $\overline{RD}$ Low		20		30		ns
5	t_{LHDV}	ALE High to Valid Data			235		285	ns
6	t_{AVDV}	Address Valid to Data Valid	3		200		250	ns
7	t_{CLDV}	$\overline{CE}$ Active to Data Valid	1,3		200		250	ns
8	t_{ELDV}	$\overline{PSEN}$ or $\overline{RD}$ Low to Data Valid	2,3		75		100	ns
9	t_{EHDX}	$\overline{PSEN}$, $\overline{RD}$, $\overline{CE}$, or Address Invalid — Whichever is first — to Data Invalid		0		0		ns
10	t_{EHDZ}	$\overline{PSEN}$ or $\overline{RD}$ High to Data High-Z	4		35		45	ns
11	t_{LLWL}	ALE Low to $\overline{WR}$ Low		20		30		ns
12	t_{WLWH}	$\overline{WR}$ Pulse Width		60		80		ns
13	t_{WHLH}	$\overline{WR}$ High to ALE High		20		30		ns
14	t_{AVWH}	Address Valid to $\overline{WR}$ High		200		250		ns
15	t_{CVWH}	$\overline{CE}$ Active to $\overline{WR}$ High		200		250		ns
16	t_{DVWH}	Data Valid to $\overline{WR}$ High		60		80		ns
17	t_{WHDX}	$\overline{WR}$ High to Data Invalid		10		20		ns
18	t_{QVEL}	Port Input Valid to $\overline{RD}$ Low		15		25		ns
19	t_{EHQX}	Data Hold after $\overline{RD}$ High		0		0		ns
20	t_{WHQV}	$\overline{WR}$ High to Port Output Valid			225		250	ns
21	t_{SVSX}	RST Pulse Width		500		500		ns
22	t_{SXAV}	RST Inactive to Address Valid		0		0		ns

NOTES:
1. t_{CLDV} is 1 μs during inteligent Identifier/NVR Mode.
2. t_{ELDV} is 750 ns during inteligent Identifier/NVR Mode.
3. Output load is 100 pF for t_{AVDV}, t_{CLDV}, and t_{ELDV}.
4. Output Load is 5 pF for t_{EHDZ}, which is measured at high-Z $\pm$500 mV.

PROGRAMMING

Caution: Exceeding 14V on V_{PP} will permanently damage the device.

Program and Data Planes

During programming (V_{PP} = 12.75V), the SFR/RAM plane is not available, only the EPROM and configuration planes (depending on PSR's value) can be accessed. The SFR/RAM plane is accessed only when V_{PP} is V_{IL} or V_{IH}.

Programming the EPROM Plane

The EPROM array is programmed if the plane select register (PSR) contains xxxxxx01b (X1h) when V_{PP} is raised to 12.75V. In an erased device, the EPROM array occupies addresses 0000h through 7FFFh and is programmed at these locations. After programming, the array can be relocated to addresses 8000h–FFFFh by programming the EPROM location register bit ELR.7 (EL) in the configuration plane. Alternately, the EPROM array can be relocated first via ELR.7 and programmed at addresses 8000h–FFFFh.

Programming the Configuration Plane

The configuration plane contains five information bytes. Addresses 0000h and 0001h contain read-only inteligent identifiers. The control level register, EPROM location register, and SFR location register are at 7FFDh, 7FFEh, and 7FFFh. These latter three non-volatile registers (NVRs) are made of EPROM cells. EPROM registers allow the device to be configured, or erased and reconfigured, for various microcontroller architectures.

These registers are programmed if the plane select register (PSR) contains xxxxxx10b (X2h) when V_{PP} is raised to 12.75V. Once this plane is entered, it is programmed and verified just like the EPROM plane.

ERASURE CHARACTERISTICS (FOR CERAMIC, WINDOWED DEVICES)

Exposure to light of wavelength shorter than 4000 Angstroms (Å) begins erasure. Sunlight and some fluorescent lamps have wavelengths in the 3000-4000Å range. Constant exposure to room-level fluorescent light can erase the EPROM array in about 3 years (about 1 week for direct sunlight). Opaque labels over the window will prevent unintentional erasure under these lighting conditions.

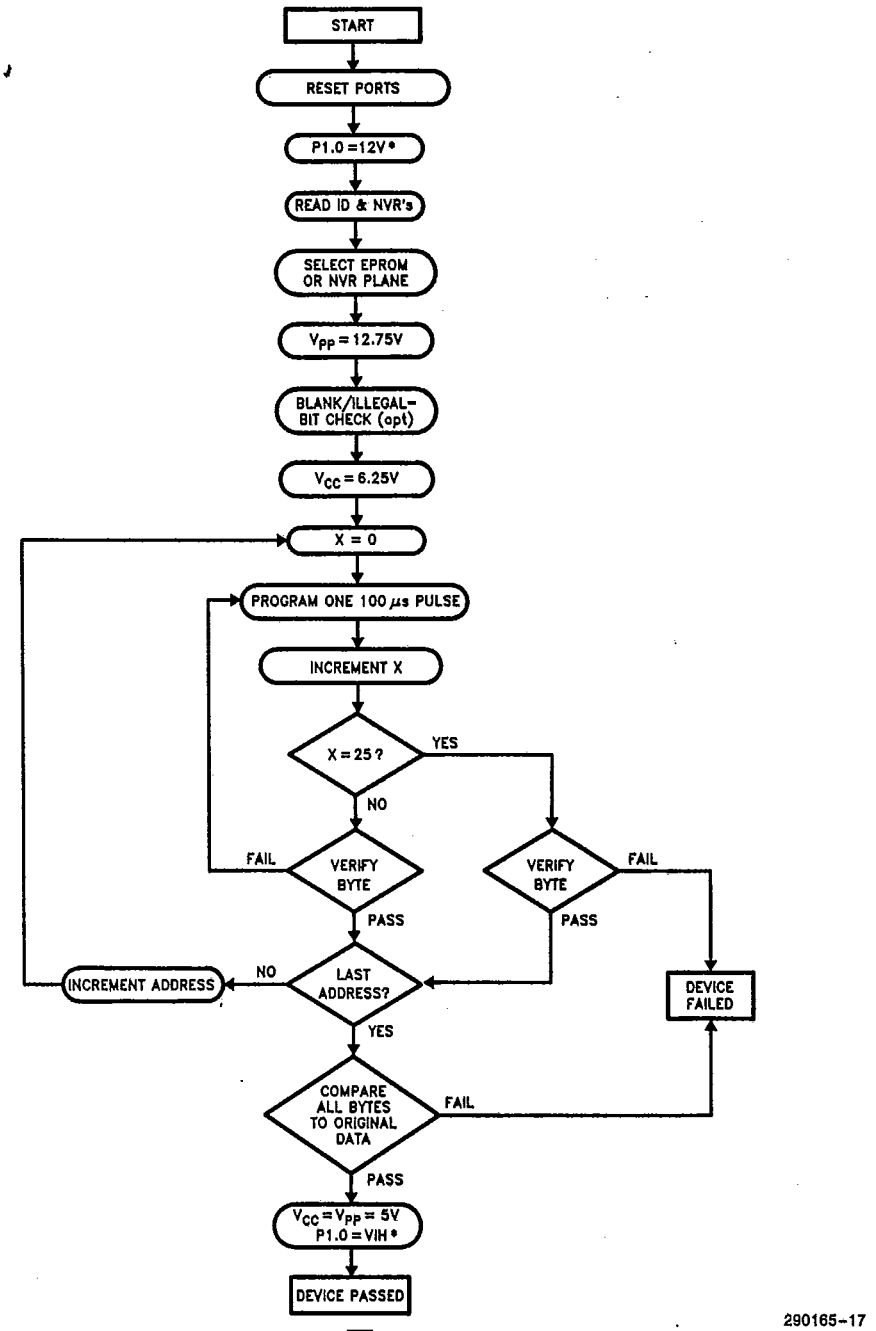
The recommended erasure procedure is exposure to 2537Å ultraviolet light. The minimum integrated Erasure time using a 12000 uW/cm^2 ultraviolet lamp is approximately 15 to 20 minutes. The EPROM should be placed about 1 inch from the lamp. The maximum integrated dose is 7258 Wsec/cm^2 (1 week - 12000 uW/cm^2). High intensity UV light exposure for longer periods can cause permanent damage.

QUICK-PULSE PROGRAMMING™ ALGORITHM

The Quick-Pulse Programming algorithm programs Intel's 87C75PF Port Expander. Developed to substantially reduce production programming throughput time, this algorithm allows optimized programming equipment to program an 87C75PF in under four seconds. Actual programming time depends on the PROM programmer used.

The Quick-Pulse Programming algorithm uses a 100 microsecond initial-pulse followed by a byte verification to determine when the addressed byte is correctly programmed. The algorithm terminates if 25 100us pulses fail to program a byte. Figure 14 shows the 87C75PF Quick-Pulse Programming algorithm flowchart.

The entire program-pulse/byte-verify and final verify sequence is performed with V_{CC} = 6.25V and V_{PP} = 12.75V. When programming is complete, all bytes should be compared to the original data with V_{CC} = 5.0V.



*P1.0 = 12V is used to internally disable the device's $\overline{RD}$ input for PROM programmers that ground this pin.

Figure 14. 87C75PF Quick-Pulse Programming™ Algorithm

D.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

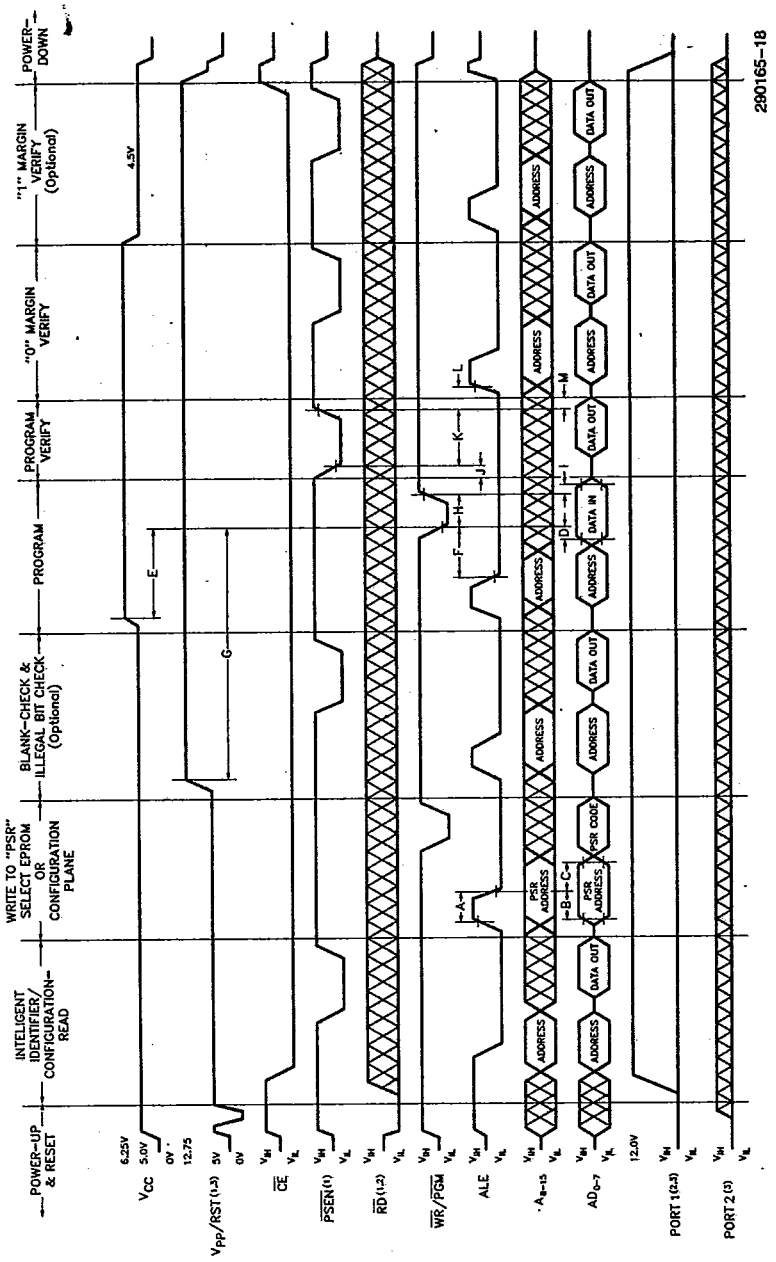
Symbol	Parameter	Notes	Min	Nominal	Max	Units	Test Conditions
I_{LI}	Input Load Current				1.0	μA	$V_{IN} = V_{IL}$ or V_{IH}
I_{CC2}	V_{CC} Supply Current	2			60	mA	$\overline{CE}$ = ALE = V_{IL}
I_{PP}	V_{PP} Supply Current	2			50	mA	$\overline{CE}$ = $\overline{WR}$ = ALE = V_{IL}
V_{IL}	Input Low Voltage		−0.5		0.8	V	
V_{IH}	Input High Voltage		2.0		$V_{CC}+0.5$	V	
V_{OL}	Verify Output Low Voltage				0.40	V	I_{OL} = 2.1 mA
V_{OH}	Verify Output High Voltage		$V_{CC}-0.8$			V	I_{OH} = −400 μA
V_{ID}	P1.0 Identifier/Configuration-Read Voltage		11.0	12.0	13.0	V	
V_{PP}	Programming Voltage	1	12.5	12.75	13.0	V	
V_{CC}	Supply Voltage During Programming	1	6.0	6.25	6.5	V	

NOTES:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum current value is with Address/Data pins AD_{0-7} in write mode; port pins are unloaded.

A.C. PROGRAMMING CHARACTERISTICS $T_A = 25°C \pm 5°C$

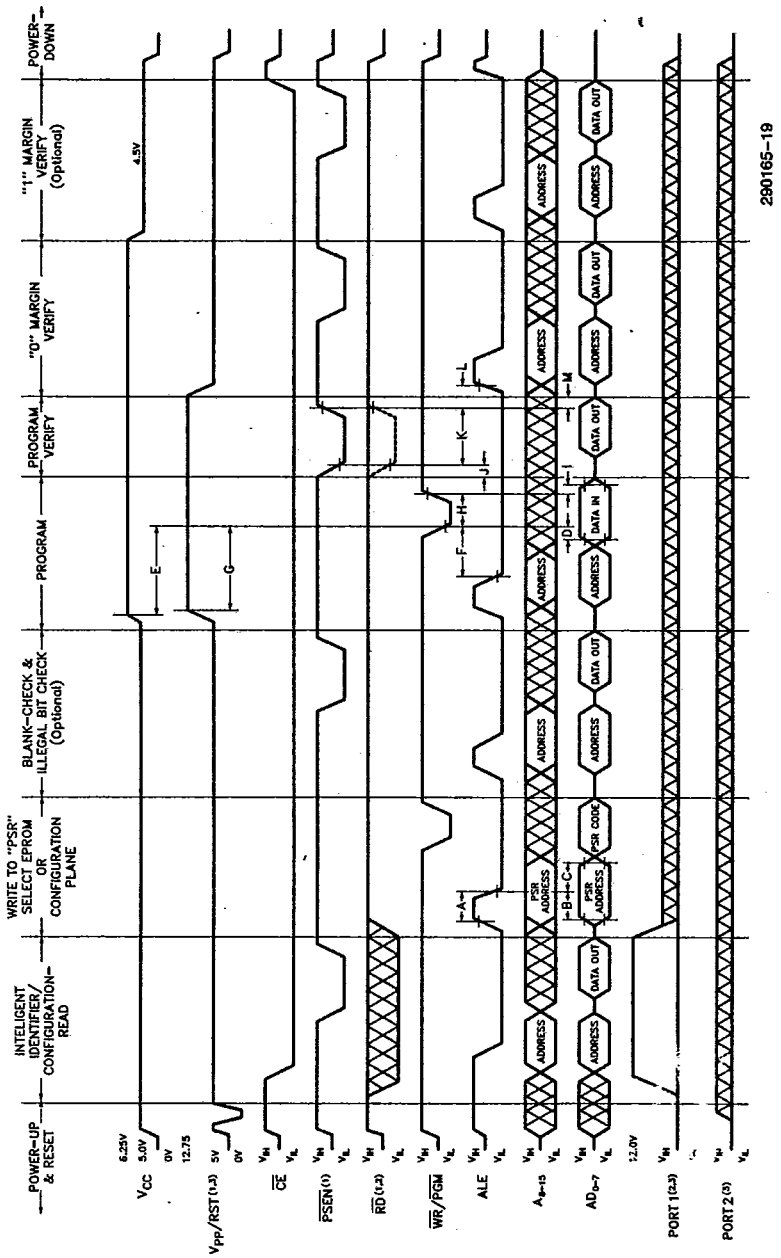
Parameter		Characteristic	Limits			Units
No	Symbol		Min	Nominal	Max	
A	t_{LHLL}	ALE Pulse Width	100			ns
B	t_{AVLL}	Address Valid to ALE Low	20			ns
C	t_{LLAX}	Address Hold after ALE Low	50			ns
D	t_{DVGL}	Data valid to $\overline{WR}/\overline{PGM}$ Low	2			μs
E	t_{CHGL}	V_{CC} Setup Time to $\overline{WR}/\overline{PGM}$ Low	2			μs
F	t_{LLGL}	ALE to $\overline{WR}/\overline{PGM}$	2			μs
G	t_{PHGL}	V_{PP} Setup Time to $\overline{WR}/\overline{PGM}$ Low	2			μs
H	t_{GLGH}	$\overline{WR}/\overline{PGM}$ Program Pulse Width	95	100	105	μs
I	t_{GHDX}	Data Hold after $\overline{WR}/\overline{PGM}$ High	2			μs
J	t_{DXEL}	Data In Float to $\overline{PSEN}$ or $\overline{RD}$ Low	2			μs
K	t_{ELEH}	$\overline{PSEN}$ or $\overline{RD}$ Verify Pulse Width	150			ns
L	t_{EHLH}	$\overline{PSEN}$ or $\overline{RD}$ High to ALE High	0			ns
M	t_{EHDZ}	$\overline{PSEN}$ or $\overline{RD}$ High to Instruction/Data High-Z	0		35	ns

PROGRAMMING WAVEFORMS (For PROM Programmers with $\overline{RD}$ = GND)



NOTES:
1. When V_{PP} = Programming Voltage, either $\overline{PSEN}$ or $\overline{RD}$ will access EPROM (if PSR = x1h) or Configuration (if PSR = x2h) Planes and inteligent Identifier mode is disabled.
2. $\overline{RD}$ is Don't-care when P1.0 = V_H.
3. Port 1 must be RESET or "1" written to P1.0 before V_H is applied to P1.0. All other Port 1 and Port 2 pins should be driven at High-Z or V_{IH} during programming.

PROGRAMMING WAVEFORMS (For PROM Programmers that can have $\overline{RD}$ = V_{IH} or V_{CC})



NOTES:
1. When V_{PP} = Programming Voltage, either $\overline{PSEN}$ or $\overline{RD}$ will access EPROM (if PSR = x1h) or Configuraton (if PSR = x2h) Planes and inteligent identifier mode is disabled.
2. $\overline{RD}$ is Don't-care when P1.0 = V_H.
3. Port 1 must be RESET or "1" written to P1.0 before V_H is applied to P1.0. All other Port 1 and Port 2 pins should be driven at High-Z or V_{IH} during programming.

REVISION HISTORY

Number	Description
04	Revised Express options. Revised catagory from ADVANCED INFORMATION to PRELIMINARY Configuration Plane—Port 2 description-**TTL** V_{OH} levels within 200 ns D.C. Characteristics—I_{CC} spec'd at **5 MHz** Programming Characteristics—V_{IL} = **−0.5V** min Programming Modes—Added intelligent identifier override description A.C. Characteristics—t_{LHDV} for -250V10 = **285** ns Improved V_{CC} tolerance to ± **10%**